

β2 region. Since the amorphous silicon is in contact with the drain and channel formation region, the depletion layer can be formed from the drain through the inside of the amorphous silicon layer. The amorphous silicon layer allows the depletion layer extending from the drain to be formed therein when the drain voltage is applied, to transmit photocarriers produced in the amorphous silicon layer to the channel forming region immediately after the production by the depletion layer.

On Page 12, Fourth Full Paragraph continuing onto Page 13, through the First Full Paragraph:

β3 A Fermi level is not necessarily located at the band gap center when forming amorphous silicon. Rather, the Fermi level shifts in a direction to form a pseudo n-type semiconductor despite no doping due to its structural problem. When the amorphous silicon is doped with p-type dopants such as boron of 3 Group and the like at 5×10^{16} to $1 \times 10^{18} \text{ cm}^{-3}$, the Fermi level can be set at the band center. The resulting amorphous silicon layer, although doped with dopants, since the location of the Fermi level is closer to an intrinsic state than that of the non-dope silicon, is considered as a substantially intrinsic state.

A transparent conductive film 1009 is formed on the amorphous silicon layer 1008. Indium tin oxide (ITO), tin oxide, and the like may be used for the film 1009. The transparent conductive film 1009 is used for application of a voltage between the source region 1007 and the film. In the present embodiment, the transparent conductive film 1009 utilizes ITO. ITO having a thickness of 1000 to 2000 Å is used considering its transmission ratio and electrical resistance value. Typically, ITO with a thickness of 1200 Å is used. ITO is material to form a Schottky junction by coupling to the amorphous silicon layer, which results in a depletion layer formed from the junction surface through the inside of the amorphous silicon layer as deep as 1000 to 3000 Å approximately by the Schottky barrier.

On Page 20, Second and Third Full Paragraphs

B4 Holding capacitor 3002 for holding electrical charges produced by photo carriers collected into a source may be separately provided or may be substituted by TFT parasitic capacitance. In the present embodiment, the holding capacitor is separately disposed. A switch TFT 3001 is used as a switch to transfer electrical charges accumulated in the holding holding capacitor to capacitor 3003. The gate of the switch TFT 3001 is coupled with a shift register for sequential application of a voltage to the shift register in synchronization with a clock.

Electrical charges in the capacity 3003 are output into an output 3006 as electrical signals through an amplifier 3005. A reset TFT 3004 is disposed between the capacitor 3003 and a ground for resetting the capacitor 3003.

On Page 21, First Full Paragraph continuing through Third Full Paragraph

B5 Holding capacitor 4002 for holding electrical charges produced by photo carriers collected into a source may be separately disposed or may be substituted by TFT parasitic capacitance. Providing the capacitor separately is more preferable. A switch TFT 4001 is used as a switch to transfer electrical charges accumulated in the holding capacitor to capacitor 4002. The gate of the switch TFT 4001 is coupled with a vertical shift register 4011, and the source or drain is coupled with a horizontal shift register 4010 through an analog switch 4009. A voltage is sequentially applied to each shift register in synchronization with a clock.

Signals transmitted through the analog switch 4009 are output into an output 4006. For a scanning method, an optical signal in the first column is output by sequentially applying a voltage to the horizontal shift register from the first to the last column while applying a voltage to the first row of the vertical shift register. Next, an optical signal in the second column is output by sequentially applying a voltage to the horizontal shift register from the first to the last column while applying a voltage to the second row of the vertical shift register. Repeating this process until the last row of the vertical shift register is applied with a voltage completes sensing of one screen.